

AMENDMENT TO THE CLAIMS

Please cancel claims 18-29 without prejudice or disclaimer;

Please amend claims 1, 3, 5, 10-12, 16, 30 and 31; and

Please add new claims 32 and 33 as follows:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A Semiconductor semiconductor structure formed on a substrate, comprising:
 - a first rigid dielectric layer;
 - a first non-rigid dielectric wiring level formed on the first rigid dielectric layer having at least one interconnect;
 - a second rigid dielectric layer formed on the first non-rigid dielectric wiring level; the interconnect being in contact with a portion of the first rigid dielectric layer and with a portion of the second rigid dielectric layer;
 - a structural securing means associated with the first non-rigid dielectric wiring level for preventing a portion, the structural securing means connecting together the portions of the first and second rigid dielectric layers above and below the first non-rigid dielectric wiring level so that the portions of the first or and second rigid dielectric layers adjacent the interconnect are prevented from de-layering from the interconnect; and
 - a low-k dielectric layer having dummy fill shapes arranged above the second rigid dielectric layer.

2. (Previously Presented) The semiconductor structure of claim 1, wherein the structural securing means comprises at least one dummy fill shape in proximity to the interconnect having a coefficient of thermal expansion better matched to the first and

second rigid dielectric layers than that of the first non-rigid dielectric wiring level.

3. (Currently Amended) The semiconductor structure of claim 2, wherein the at least one dummy fill shape is ~~one of~~ an alloy predominately composed of one of copper, aluminum and tungsten.

4. (Previously Presented) The semiconductor structure of claim 2, wherein an effective CTE of a region of the first non-rigid dielectric wiring level is reduced in proportion to a density of the at least one dummy fill shape.

5. (Currently Amended) The semiconductor structure of claim 1, wherein the structural securing means ~~are~~ is a plurality of dummy fill shapes aligned in rows and columns about the interconnect.

6. (Original) The semiconductor structure of claim 1, wherein the structural securing means is matched to an overall average local metal density such that CTE mismatch stresses and deflections are substantially toward zero.

7. (Original) The semiconductor structure of claim 1, wherein the structural securing means reduces temperature-driven stress.

8. (Previously Presented) The semiconductor structure of claim 1, wherein the structural securing means inhibits deflecting of the first and second rigid dielectric layers.

9. (Previously Presented) The semiconductor structure of claim 1, wherein:
the interconnect has a line width from 0.1 microns to greater than 1 micron;
the structural securing means are dummy fill shapes adjacent to the interconnect;

the dummy fill shapes are one of an alloy substantially composed of aluminum, copper and tungsten; and

the dummy fill shapes are electrically isolated from each other and the interconnect.

10. (Currently Amended) ~~The semiconductor structure of claim 9, A~~
semiconductor structure formed on a substrate, comprising:

a first rigid dielectric layer;

a first non-rigid dielectric wiring level formed on the first rigid dielectric layer
having at least one interconnect;

a second rigid dielectric layer formed on the first non-rigid dielectric wiring level;
dummy fill shapes associated with the first non-rigid dielectric wiring level for
preventing a portion of the first or second rigid dielectric layers adjacent the
interconnect from de-layering from the interconnect;

a low-k dielectric layer having dummy fill shapes arranged above the second
rigid dielectric layer;

the interconnect having a line width from 0.1 microns to greater than 1 micron;
and

the dummy fill shapes being adjacent to the interconnect, being an alloy
substantially composed of one of aluminum, copper and tungsten, and being electrically
isolated from each other and the interconnect,

wherein a minimum spacing between the dummy fill shapes are one to four times a ~~maximum minimum~~ spacing for ordinary wires on the first non-rigid dielectric wiring level.

11. (Currently Amended) ~~The semiconductor structure of claim 9, A~~
semiconductor structure formed on a substrate, comprising:

a first rigid dielectric layer;

a first non-rigid dielectric wiring level formed on the first rigid dielectric layer

having at least one interconnect;

a second rigid dielectric layer formed on the first non-rigid dielectric wiring level;
dummy fill shapes associated with the first non-rigid dielectric wiring level for
preventing a portion of the first or second rigid dielectric layers adjacent the
interconnect from de-layering from the interconnect;

a low-k dielectric layer having dummy fill shapes arranged above the second
rigid dielectric layer;

the interconnect having a line width from 0.1 microns to greater than 1 micron;
and

the dummy fill shapes being adjacent to the interconnect, being an alloy
substantially composed of one of aluminum, copper and tungsten, and being electrically
isolated from each other and the interconnect,

wherein a minimum spacing between the dummy fill shapes are is equal to a
minimum spacing width for ordinary wires on the first non-rigid dielectric wiring level.

12. (Currently Amended) ~~The semiconductor structure of claim 9, A~~
semiconductor structure formed on a substrate, comprising:

a first rigid dielectric layer;
a first non-rigid dielectric wiring level formed on the first rigid dielectric layer
having at least one interconnect;
a second rigid dielectric layer formed on the first non-rigid dielectric wiring level;
dummy fill shapes associated with the first non-rigid dielectric wiring level for
preventing a portion of the first or second rigid dielectric layers adjacent the
interconnect from de-layering from the interconnect;

a low-k dielectric layer having dummy fill shapes arranged above the second
rigid dielectric layer;

the interconnect having a line width from 0.1 microns to greater than 1 micron;
and

the dummy fill shapes being adjacent to the interconnect, being an alloy

substantially composed of one of aluminum, copper and tungsten, and being electrically isolated from each other and the interconnect,

wherein a density of the dummy fill shapes is between approximately 45% and 50%.

13. (Original) The semiconductor structure of claim 9, wherein a width and length of the dummy fill shapes are 3x a minimum line width of the interconnect.

14. (Original) The semiconductor structure of claim 1, wherein the structural securing means are dummy fill shapes arranged in a staggered offset pattern surrounding the interconnect.

15. (Original) The semiconductor structure of claim 1, wherein the first non-rigid dielectric wiring level is a low-k dielectric siloxane based semi-organic layer.

16. (Currently Amended) The semiconductor structure of claim 15, wherein the first and second rigid dielectric layer layers contains silicon oxide based glass.

17. (Original) The semiconductor structure of claim 1, wherein the structural securing means are a plurality of square shaped dummy fill shapes arranged in a staggered pattern in the first non-rigid dielectric wiring level.

Claims 18-29 (Canceled).

30. (Currently Amended) A process of forming a semiconductor structure, comprising:

forming a first rigid dielectric layer;

forming a first non-rigid dielectric wiring level on the first rigid dielectric layer having an interconnect;

forming a second rigid dielectric layer on the first non-rigid dielectric wiring level;
and

forming a plurality of dummy metal fill shapes in the first non-rigid dielectric wiring level in proximity to the interconnect ~~for, wherein the interconnect is in contact with a portion of the first rigid dielectric layer and with a portion of the second rigid dielectric layer; and~~

~~preventing, with the dummy metal fill shapes, the portions a portion of the first or and second rigid dielectric layers adjacent the interconnect from de-layering away from the interconnect.~~

31. (Currently Amended) ~~The process of claim 30,~~ A process of forming a semiconductor structure, comprising:

forming a first rigid dielectric layer;

forming a first non-rigid dielectric wiring level on the first rigid dielectric layer having an interconnect;

forming a second rigid dielectric layer on the first non-rigid dielectric wiring level;
and

forming a plurality of dummy metal fill shapes in the first non-rigid dielectric wiring level in proximity to the interconnect for preventing a portion of the first or second rigid dielectric layers adjacent the interconnect from de-layering away from the interconnect,

wherein the forming of the plurality of dummy fill shapes includes forming a density of approximately 45% to 50%.

32. (New) The process of claim 30, wherein the preventing comprises physically connecting together, with the dummy metal fill shapes, the first and rigid dielectric layers above and below the first non-rigid dielectric wiring level, and wherein the dummy metal fill shapes are electrically isolated from each other.

33. (New) The semiconductor structure of claim 1, wherein the structural securing means comprises a plurality of dummy metal fill shapes which are electrically isolated from each other and wherein the plurality of dummy metal fill shapes physically connect together the first and rigid dielectric layers adjacent the interconnect.